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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,427	09/28/2006	Seiichi Tamura	03500.109226.	8692

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NEW YORK, NY 10104-3800

EXAMINER
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CHIU, TSZ K

ART UNIT	PAPER NUMBER
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2822

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11/27/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/599,427	<b>Applicant(s)</b> TAMURA ET AL.	
	<b>Examiner</b> Tsz K. Chiu	<b>Art Unit</b> 2822	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 5-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9 is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 1,2 and 5-8 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Isogai et al. (20010000068).

With respect to claim 1, Isogai discloses:

a plurality of pixels (shown in figure 11) arranged in a pixel region (See drawing below), each pixel including a photoelectric conversion (1, For example fig. 1 or fig. 46) region for converting light into signal charge (paragraph 28), a transfer transistor (5,15,18 For example Fig. 46) for transferring the signal charge from the photoelectric conversion region; and

a peripheral circuit (See drawing below) arranged outside of the pixel region (See drawing below) and including a circuit for processing the signal charge (paragraph 28),

wherein the plurality of pixels (shown in figure 11) and the peripheral circuit (See drawing below) are disposed together on a substrate (10, For example Fig. 46)

wherein the pixel region (region of 1, For example fig. 1 or fig. 46) includes

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a first semiconductor region (14, For example Fig. 46) of a first conductivity type (N type) disposed in the substrate (10, For example Fig. 46) of a second conductivity type (P type) that is opposite to the first conductivity type (N type);

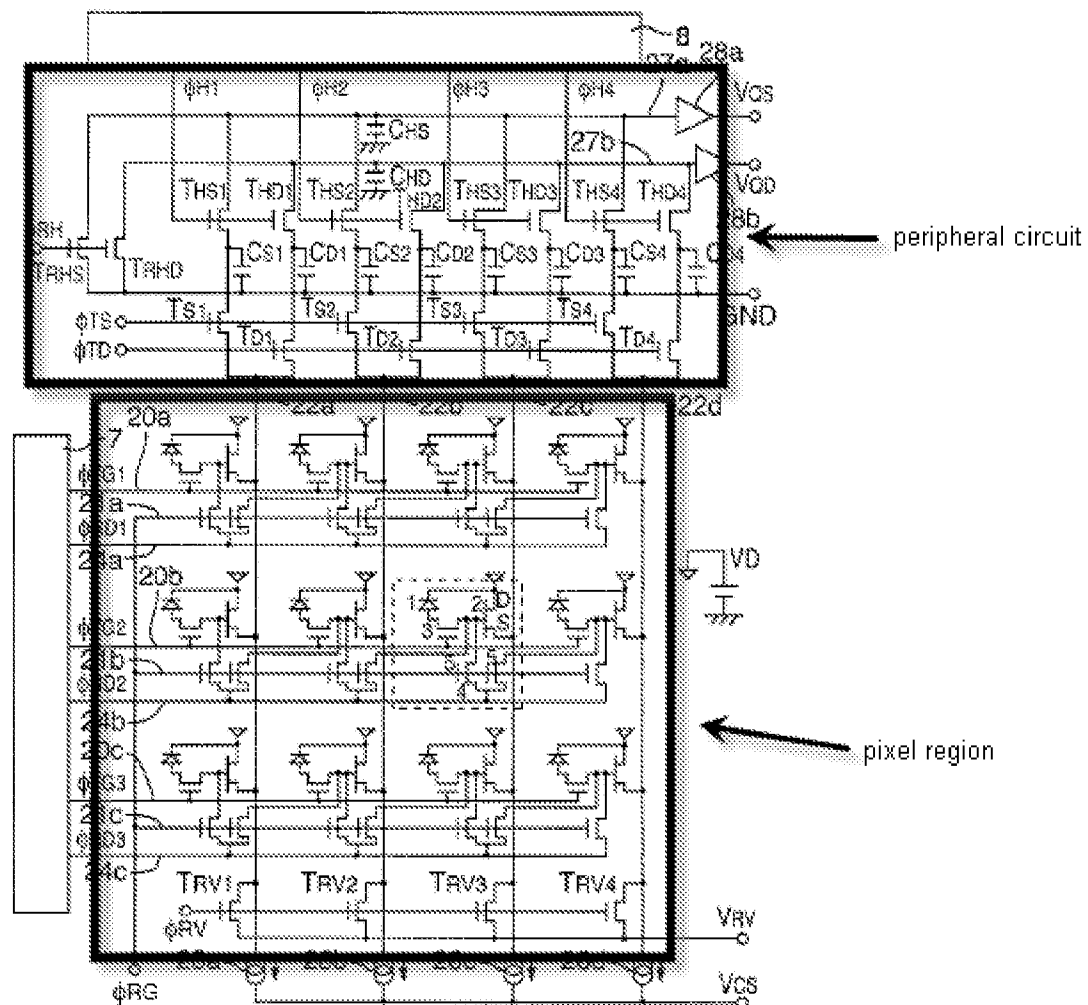
a second semiconductor region (15, For example Fig. 46) of the second conductivity type (P type) disposed in the substrate (10, For example Fig. 46) the signal charge (paragraph 28), and

the transfer transistor (5,15,18 For example Fig. 46) disposed in the first semiconductor region (14, For example Fig. 46),

wherein the peripheral circuit (See drawing below) includes a third semiconductor region (11, For example Fig. 46) of the first conductivity type (N type); disposed in the substrate (10, For example Fig. 46), such that a transistor forming the peripheral circuit is arranged in the third semiconductor region,

wherein an impurity concentration of the first semiconductor region (14, For example Fig. 46) is higher than an impurity concentration of the third semiconductor region (11, For example Fig. 46), and

wherein the first semiconductor region (14, For example Fig. 46) extends deeper into the substrate (10, For example Fig. 46) than the third semiconductor region (11, For example Fig. 46).



With respect to claim 2, Isogai discloses

a plurality of pixels (shown in figure 11) arranged in a pixel region (See drawing below), each pixel including a photoelectric conversion (1, For example fig. 1 or fig. 46) region for converting light into signal charge (paragraph 28), and a transfer transistor (5,15,18 For example Fig. 46) for transferring the signal charge from the photoelectric conversion region; and

a peripheral circuit (See drawing below) arranged outside of the pixel region (See drawing below) and including a circuit for processing the signal charge (paragraph 28),

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wherein the plurality of pixels (shown in figure 11) and the peripheral circuit (See drawing below) are disposed together on a substrate (10, For example Fig. 46),

wherein the pixel region (region of 1, For example fig. 1 or fig. 46) includes:

a first semiconductor region (14, For example Fig. 46) of a first conductivity type (N type) disposed in the substrate (10, For example Fig. 46), the substrate (10, For example Fig. 46) being of a second conductivity type (P type) that is opposite to the first conductivity type;

a second semiconductor region (15, For example Fig. 46) of the second conductivity type (P type) disposed in the substrate (10, For example Fig. 46) such that the first semiconductor region (14, For example Fig. 46) and second semiconductor region (15, For example Fig. 46) accumulate the signal charge (paragraph 28); and

the transfer transistor (5,15,18 For example Fig. 46) disposed in the first semiconductor region (14, For example Fig. 46),

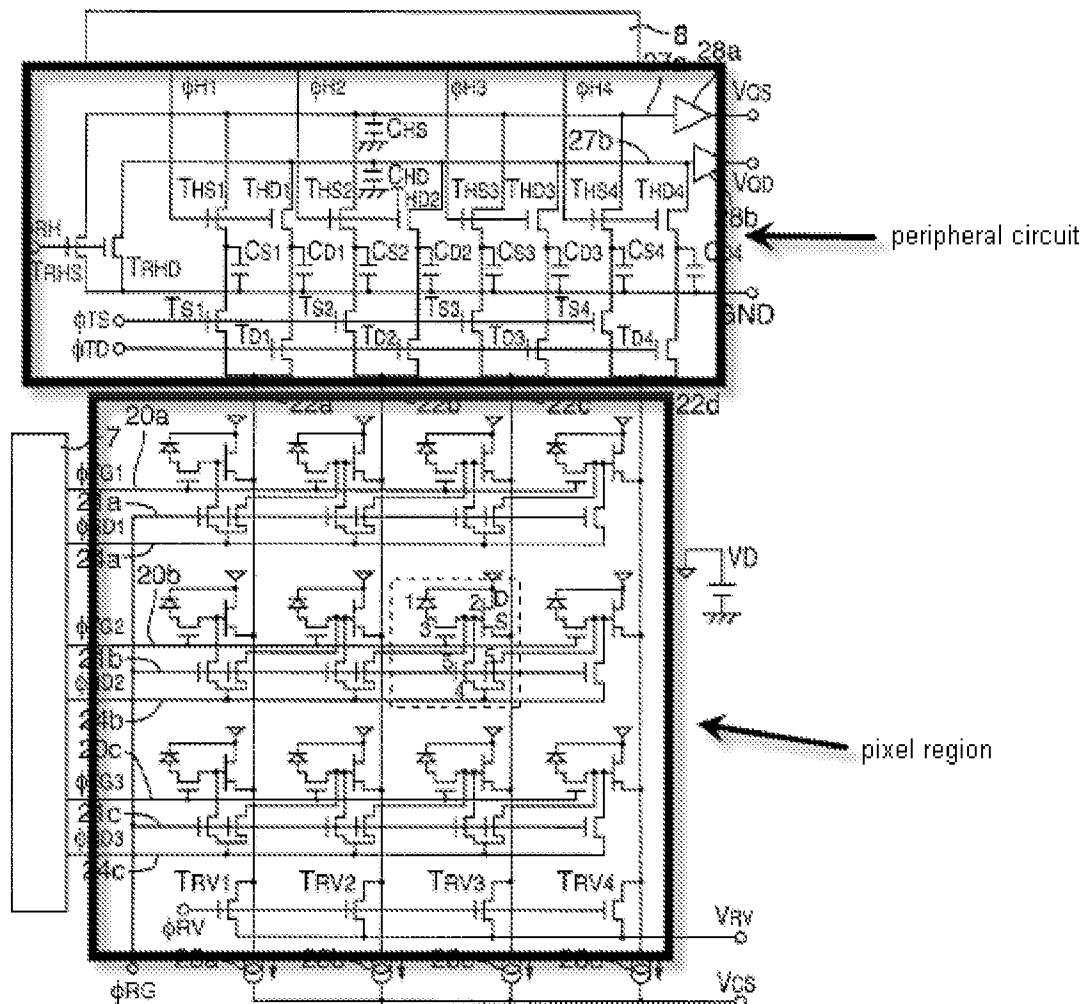
wherein the peripheral circuit (See drawing below) includes a third semiconductor region (11, For example Fig. 46) of the first conductivity type (N type) disposed in the substrate (10, For example Fig. 46), such that a transistor forming the peripheral circuit is arranged in the third semiconductor region,

wherein said first and third semiconductor region (11, For example Fig. 46)s have impurity concentration profiles forming peaks,

wherein a peak impurity concentration of the first semiconductor region (14, For example Fig. 46) is higher than a peak impurity concentration of the third semiconductor region (11, For example Fig. 46), and

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wherein the peak impurity concentration position of the first semiconductor region (14, For example Fig. 46) is disposed deeper than the peak impurity concentration of the third semiconductor region (11, For example Fig. 46).



With respect to claim 5, Isogai discloses

wherein the first semiconductor region (14, For example Fig. 46) has a structure wherein plural semiconductor regions have impurity concentration peaks disposed in a depth direction inside the substrate (10, For example Fig. 46), and

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an impurity concentration of an impurity concentration peak disposed in a deepest portion is higher than an impurity concentration of an impurity concentration peak disposed at a side of the photoelectric conversion (1, For example fig. 1 or fig. 46) device.

With respect to claim 6, Isogai discloses

Wherein the first semiconductor region (14, For example Fig. 46) and the third semiconductor region (11, For example Fig. 46) are formed of plural semiconductor region having impurity concentration peaks, and a peak impurity concentration of a region of a highest impurity concentration peak, among plural regions of the first semiconductor region (14, For example Fig. 46), is higher than a peak impurity concentration of a region of a highest impurity concentration peak concentration among plural regions of the third semiconductor region (11, For example Fig. 46).

With respect to claim 7, Isogai discloses

a plurality of pixels (shown in figure 11) arranged in a pixel region (See drawing below), each pixel including a photoelectric conversion (1, For example fig. 1 or fig. 46) region for converting light into signal charge (paragraph 28), and a transfer transistor (5,15,18 For example Fig. 46) for transferring the signal charge from the photoelectric conversion region; and

a peripheral circuit (See drawing below) arranged outside of a pixel region (See drawing below), the peripheral circuit (See drawing below) including a circuit for processing the signal charge (paragraph 28),



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wherein the pixels and peripheral circuit (See drawing below) are disposed together on a substrate (10, For example Fig. 46),

wherein the pixel region (region of 1, For example fig. 1 or fig. 46) includes:

a first semiconductor region (14, For example Fig. 46) of a first conductivity type (N type) disposed in the substrate (10, For example Fig. 46) of a second conductivity type (P type) that is opposite to the first conductivity type (N type);

a second semiconductor region (15, For example Fig. 46) of the second conductivity type (P type) disposed in the substrate (10, For example Fig. 46) such that the first semiconductor region (14, For example Fig. 46) and second semiconductor region (15, For example Fig. 46) accumulate the signal charge (paragraph 28); and

the transfer transistor (5,15,18 For example Fig. 46) disposed in the first semiconductor region (14, For example Fig. 46),

wherein the peripheral circuit (See drawing below) includes:

a third semiconductor region (11, For example Fig. 46) of the first conductivity type (N type) disposed in the substrate (10, For example Fig. 46), such that a transistor forming the peripheral circuit is arranged in the third semiconductor region,

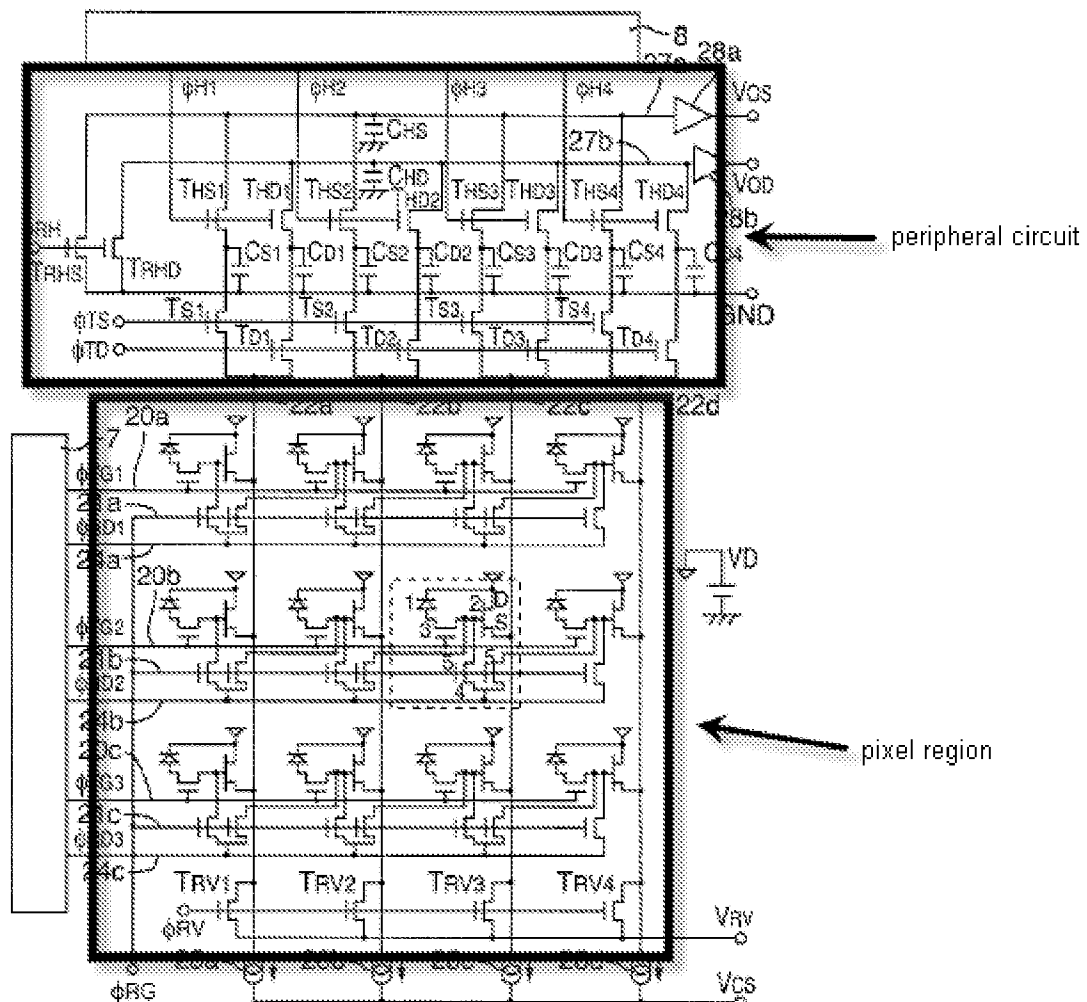
wherein the first semiconductor region (14, For example Fig. 46) has a structure wherein plural semiconductor regions having impurity concentration peaks are disposed in a depth direction inside the substrate (10, For example Fig. 46),

wherein an impurity concentration of an impurity concentration peak disposed in a deepest portion is higher than an impurity concentration of an impurity concentration

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peak disposed at a side of the photoelectric conversion (1, For example fig. 1 or fig. 46) device, and

wherein impurity concentration of an impurity concentration peak disposed in a deepest portion of the first semiconductor region (14, For example Fig. 46) is higher than an impurity concentration of an impurity concentration peak of the third semiconductor region (11, For example Fig. 46).



With respect to claim 8, Isogai discloses

wherein the impurity concentration peak disposed in the deepest portion of the first semiconductor region (14, For example Fig. 46) is deeper than an impurity concentration peak of the third semiconductor region (11, For example Fig. 46) .

***Allowable Subject Matter***

Claim 9 allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claim 9 is allowable over the reference of record because none of these references discloses or can be combined to yield the claimed invention of a photoelectric conversion device having a first semiconductor region of a first conductivity type disposed in the substrate of a second conductivity type that is opposite to the first conductivity type;

a second semiconductor region of the second conductivity type disposed in the first semiconductor region, being a part of the photoelectric conversion region and accumulating the signal charge, and

a third semiconductor region serving as a well of the first conductivity type disposed in the substrate, and

source and drain region of a transistor forming the peripheral circuit, wherein an impurity concentration of the first semiconductor region is higher than an impurity concentration of the third semiconductor region, and

wherein the first semiconductor region extends deeper into the substrate than the third semiconductor region.

Therefore claim 9 is allowable.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/  
Supervisory Patent Examiner, Art  
Unit 2822

/Tsz K Chiu/  
Examiner, Art Unit 2822  
November 21, 2009